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Application : 10/045927 **Examiner :** Moazzami **GAU :** 2187

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REV 10/04

Method And Apparatus For Using Global Snooping To Provide Cache Coherence To Distributed Computer Nodes In A Single Coherent System

Cross-Reference to Related Applications

The following patent applications, all assigned to the assignee of this application, describe related aspects of the arrangement and operation of multiprocessor computer systems according to this invention or its preferred embodiment.

U.S. patent application serial number 10/045,798 by T. B. Berg et al. (BEA919990003US1) entitled "~~Method And Apparatus For Increasing Requestor~~ Increased Computer Peripheral Throughput By Using Data Available Withholding" was filed on January 9, 2002.

U.S. patent application serial number 10/045,821 by T. B. Berg et al. (BEA920000018US1) entitled "Multi-level Classification Method For Transaction Address Conflicts For Ensuring Efficient Ordering In A Two-level Snoopy Cache Architecture" was filed on January 9, 2002.

U.S. patent application serial number 10/045,564 by S.G. Lloyd et al. (BEA920000019US1) entitled "Transaction Redirection Mechanism For Handling Late Specification Changes And Design Errors" was filed on January 9, 2002.

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U.S. patent application serial number 10/045,797 by T. B. Berg et al. (BEA920000020US1) entitled "Method And Apparatus For Multi-path Data Storage And Retrieval" was filed on January 9, 2002.

U.S. patent application serial number 10/045,923 by W. A. Downer et al. (BEA920000021US1) entitled "Hardware Support For Partitioning A Multiprocessor System To Allow Distinct Operating Systems" was filed on January 9, 2002.

U.S. patent application serial number 10/045,925 by T. B. Berg et al. (BEA920000022US1) entitled "Distributed Allocation Of System Hardware Resources For Multiprocessor Systems" was filed on January 9, 2002.

U.S. patent application serial number 10/045,926 by W. A. Downer et al. (BEA920010030US1) entitled "Masterless Building Block Binding To Partitions" was filed on January 9, 2002.

U.S. patent application serial number 10/045,774 by W. A. Downer et al. (BEA920010031US1) entitled "Building Block Removal From Partitions" was filed on January 9, 2002.

U.S. patent application serial number 10/045,796 by W. A. Downer et al. (BEA920010041US1) entitled "Masterless Building Block Binding To Partitions Using Identifiers And Indicators" was filed on January 9, 2002.

Background Of The Invention

Technical Field

The present invention relates generally to computer data cache schemes, and more particularly to a method and apparatus for maintaining coherence between memories within a system having distributed shared memory when such system utilizes multiple data processors capable of being configured into separate, independent nodes in a system utilizing non-uniform memory access (NUMA) or system memory which is distributed across various nodes.

Description of the Related Art

In computer system designs utilizing more than one processor operating simultaneously in a coordinated manner, system memory which may be physically configured or associated with one group of such processors is accessible to other processors or processor groups in such system. Because of the demand for greater processing power within data processing systems, and due to the desire to have relatively small microprocessors work cooperatively sharing system components as a multi-processing system, there have been many attempts over the last several years to solve the problems inherent in maintaining coherence between memory devices which are accessible to more than one processing device or more than one system